AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A comparator outputting one bit digital signal after comparing two analog input signals by alternately performing a track mode operation and a latch mode operation decided according to a clock signal ~~having a constant period~~, the comparator comprising:

a differential input unit ~~inputting~~ for receiving the two analog input signals~~,~~ ~~wherein the two analog input signals are treated as a different input~~ and outputting a differential output;

a tracking/latching unit ~~respectively performing a tracking and latching operation through receiving a differential output of the differential input unit from an ordinary/sub input terminal and having a different current pass from each of the ordinary/sub input terminal of the tracking/latching unit itself in order to make the tracking/latching unit itself operated as a load of the differential input unit for a tracking operation in the track mode~~ for receiving the differential output through a main input terminal and a sub input terminal of the tracking/latching unit in order to perform the track mode operation and the latch mode operation according to the clock signal; and

a first latching unit for latching and outputting an output of the tracking/latching unit;

wherein each of the main input terminal and the sub input terminal has a different current pass for having a constant gain of the comparator during the track mode operation.

2. (Currently Amended) The comparator as recited in claim 1, wherein the tracking/latching unit includes:

a second latching unit having the ~~main/sub~~ main input terminal and the sub input terminal;

a first switching transistor having the clock signal as a gate input and having one end coupled to the main input terminal;

a first load transistor which is diode-connected ~~to~~ between the other end of the first switching transistor and ~~a~~ ground ~~end~~;

a second switching transistor having a gate receiving the clock signal as a gate input and one end coupled to the sub input terminal; and

a second load transistor which is diode-connected ~~to~~ between the other end of the second switching transistor and ~~to the other end of the~~ ground ~~terminal~~.

3. (Original) The comparator as recited in claim 2, wherein the first load transistor and the second load transistor are large enough to neglect the first switching transistor and the second switching transistor, respectively.

4. (Currently Amended) The comparator as recited in claim 3, wherein size of the first switching transistor is identical to that of the second switching transistor and size of the first load transistor is identical to that of ~~that of~~ the second switching transistor.

5. (Currently Amended) The comparator as recited in claim 2, wherein the second latching unit includes a first transistor and a second transistor ~~having~~ whose gates are cross-connected to the main input terminal and the sub input terminal, respectively.

6. (Currently Amended) The comparator as recited in claim 1, wherein the ~~CMOS~~ comparator further includes a switching unit ~~for switching~~ in order to connect or disconnect ~~between~~ the first latching unit with the tracking/latching unit in response to the clock signal.

7. (Currently Amended) The comparator as recited in claim 6, wherein the switching unit includes a third switching transistor and a fourth switching transistor ~~having a gate receiving~~ whose gates receive the clock signal, ~~and forming a source-drain by connecting the main/sub terminals of the tracking/latching means and the latch means~~ wherein the third switching transistor is connected between the first latching unit and the main input terminal and the fourth switching transistor is connected between the first latching unit and the sub input terminal.